WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Sunday, March 19, 2006

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
☐	L8	L1 and ((boron or arsenic) with (dopant or doped))	70
☐	L7	trench and (p near doped) and (rins$4 with acetone)	14
☐	L6	L4 and ((boron or arsenic) with (dopant or doped))	27
☐	L5	L4 and ((As or Ga or In or P) with doped)	35
☐	L4	trench and (dopant$4 or doped) and (rins$4 with acetone)	71
☐	L3	collar and (dopant$4 or doped) and (rins$4 with acetone)	5
☐	L2	(dopant$4 ion$2) and (rins$4 with acetone)	26
☐	L1	dopant$4 and (rins$4 with acetone)	352

END OF SEARCH HISTORY

L6: Entry 27 of 27 File: USPT Sep 17, 1985

DOCUMENT-IDENTIFIER: US 4541168 A
TITLE: Method for making metal contact studs between first level metal and regions of a semiconductor device compatible with polyimide-filled deep trench isolation schemes

Abstract Text (1):
The present method discloses the steps to form metal device contact studs between regions of a semiconductor device, such as an NPN vertical bipolar transistor, and the first level metal, the studs overlapping both a contact region (such as the base or the collector) and an adjacent polyimide-filled trench. The method is comprised of the following steps:

Abstract Text (2):
(a) applying a lift off mask exposing said contact region and adjacent trench without attacking the polyimide fill,

Brief Summary Text (3):
The present invention relates to the manufacture of high performance VLSI semiconductor chips in general and more particularly to a lift-off method for making metal contact studs between first level metal and the desired regions of polyimide-filled deep trench-isolated devices, typically bipolar NPN transistors.

Brief Summary Text (5):
Recent developments of advanced semiconductor devices, such as bipolar transistors, have been executed using polysilicon base contacts in conjunction with shallow junctions. There is also a strong tendency to extensively use the polyimide-filled deep trench isolation for denser integration.

Brief Summary Text (6):
Although the polysilicon base contact reduces Ccb and Rb, it adds additional topology steps (0.7 .mu.m) to the master slice structure. Moreover, standard manufacturing techniques of polyimide-filled deep trench isolated devices generally reduce trench widths to a minimum. With conventional metallurgical schemes using the so called first level metal technique, this results in increased metal land capacitance (first level metal to substrate). It also results in primary technology problems of metal thinning (edge coverage) at or over abrupt trench isolation steps and, parasitic FETs which can occur when first level metal conductors lie over thin field dielectrics.

Brief Summary Text (9):
However, none of the stud contacting art known to the present applicant is directed to semiconductor devices manufactured according to the polyimide-filled deep trench isolation technology. Standard oxygen Reactive Ion Etching (RIE) cannot be used directly with that technology, because the polyimide fill is attached. Furthermore, forming the contact studs using metal RIE or wet sub-etch processes, result in residual metal rails (caused by the anisotropy of this type of etching) or excessive process bias, respectively.

Brief Summary Text (10):
In addition, the problem of implementing metal contact studs overlapping the contact regions and the surface of the trenches adjacent thereto, in order to increase density by alleviating misregistration concerns, has not been addressed at all up to now.

Brief Summary Text (12):
Therefore it is a primary object of the invention to provide a method for making metal contact studs between first level metal and desired contact regions of a polyimide-filled deep trench isolated device which is not detrimental to the polyimide integrity.

Brief Summary Text (13):
It is another object of the invention to provide a method for making metal contact studs to the desired regions (e.g. base and collector regions) abutted to the trenches of a polyimide-filled deep trench-isolated device (e.g. a bipolar NPN vertical transistor).

Brief Summary Text (14):
It is still another object of the invention to provide a method for making metal contact studs between first level metal and desired contact regions of a polyimide-filled deep trench-isolated device which includes the step of integrating a metal diffusion barrier between the studs and the contact regions for increased reliability of the device.

Brief Summary Text (15):
It is still another object of the invention to provide a method for making metal contact studs between first level metal and desired contact regions of a polyimide filled deep trench-isolated device which includes the step of argon polishing to leave a substantially planarized structure.

Brief Summary Text (16):
It is still another object of the invention to provide a method for making metal contact studs between first level metal and desired metal contacts of a polyimide-filled deep trench semiconductor device which, on the one hand, reduces first level metal to substrate capacitance and, on the other hand, eliminates both metal thinning due to etch back variations of trench fill materials and parasitic FETs problems associated with first level metal running over thin field dielectric films.

Brief Summary Text (18):
The present invention is a method for making metal contact studs to desired contact regions of active and/or passive semiconductor devices which is fully compatible with the polyimide-filled deep trench technology. First metal interconnections are made to the metal stud instead of directly to the device. As a consequence, the first level metal lands run over a uniform, relatively thick (1.0-2.0 .mu.m), dielectric layer of an insulating material such as silicon nitride, sputtered silicon dioxide, and combination thereof, polyimide, and the like.

Brief Summary Text (19):
A standard manufacturing process is followed until the trench fill and etch back steps have been completed.

Brief Summary Text (21):
(a) applying a lift-off mask exposing desired regions, including at least one contact region abutting a trench, without attacking organic fill,

Drawing Description Text (2):
FIG. 1 shows a schematical cross sectional view of a prior art advanced bipolar NPN transistor structure after all master slice processing steps have been completed,

including polyimide fill of isolation trenches.

Detailed Description Text (2):
In the following description, the present invention is described with reference to the fabrication process of a standard advanced integrated circuit where the only active device to be formed is a bipolar transistor, whose isolation is effected by polyimide-filled deep trenches. It should be understood, of course, that various other embodiments of the present invention are realizable.

Detailed Description Text (4):
FIG 1 shows, as a non-limiting example, a vertical NPN bipolar transistor isolated by polyimide-filled deep trenches. Other devices, such as diodes, and resistors, for example, also could be provided but are not shown in the interest of clarity of exposition.

Detailed Description Text (5):
The structure 10 is comprised of a p.sup.- boron doped substate 11 having a blanket N.sup.+ subcollector 12 and an N.sup.- epitaxial layer 13 thereon. The latter includes a conventional NPN transistor structure comprised of: an N.sup.+ reach-through 14, a P base region 15 and an N.sup.+ emitter region 16. The structure is passivated with a composite insulating layer of SiO.sub.2 (.perspectiveto.300 nm) and Si.sub.3 N.sub.4 (.perspectiveto.100 nm) respectively referenced 17 and 18. The thickness irregularities of both layers, which are representative of the thermal history of the chip during the prior processing steps, have not been represented here for sake of clarity. The silicon nitride layer acts as an oxidation barrier mask to protect the top surface during trench sidewall oxidation. Trenches 19 have been formed through the structure until substrate 11 has been reached. As known, the trenches define isolated pockets of portions of the epitaxial layer where active and/or passive devices are formed.

Detailed Description Text (6):
A thermally grown SiO.sub.2 layer 20 (50-150 nm) and a Chemical Vapor Deposited Si.sub.3 N.sub.4 layer 21, coat the trench sidewalls. There is a channel stopper 22 at the bottom of the trenches to prevent undesirable effects caused by channel inversion between the subcollectors of two adjacent pockets.

Detailed Description Text (7):
The trenches are filled with an organic insulating material, such as polyimide, bearing reference 23 in FIG. 1. All the required contact openings have been etched through the composite SiO.sub.2 /Si.sub.3 N.sub.4 layer. The contact openings with the base, emitter and collector regions of structure 10 are respectively reference 24, 25 and 26. It is common practice that platinum-silicide (Pt-Si) be formed in these contact regions for improved interconnection. It is very important to understand that, at this stage the top surface of the polyimide-filled trenches 19 is exposed. The topology at the locations where the contact regions abut the trenches result from a prior back etch step. From that stage, the process proceeds as described in the following steps:

Detailed Description Text (9):
A special lift-off process has been developed to delineate the desired stud opening pattern without attacking the underlying polyimide. The wafers are first cleaned in acetone for 5 min., then rinsed, and dried. An adhesion promoter, such as Hexa-Methyl-DiSilazane (HMDS) is applied, then baked at 160.degree. C. for 30 min. A photoresist such as the diazo resist AZ 1350J, with 1% imidazole is deposited onto the structure to form a 3 .mu.m thick layer 27. The wafer is baked at 80.degree. C. for 30 min., and then is exposed to the desired pattern. After a post-exposure bake at 90.degree. C. for 20 min., the image is developed with an image stripper which selectively removes the photoresist but is inactive with the polyimide. A potassium hydroxide (KOH) solution at 0.095N is appropriate. Over developing is necessary to fully clean the contact regions and assure that the sidewalls of the mask will have

a negative profile as shown to exhibit the desired undercut required for a secure metal deposition. The polyimide acts as an etch stopper.

Detailed Description Text (13):
The wafer is dipped in an N-Methyl-Pyrrolidone (NMP) or any other suitable solvent bath at 135.degree. C. and agitated for 2 min. Then, the wafer is successively dipped in acetone for 10 min, in a resist stripper such as J 100 (a solvent sold by Indust-RI-Chemical Laboratory Inc., Richardson, Texas) for 15 min. at 98.degree. C., and in acetone for 10 min. The wafer is then rinsed and spin dried. All the metal is removed with the lift-off structure, except the device contact studs.

Detailed Description Text (14):
It is to be noted, as apparent from FIG. 4, that there are two categories of contacts: normal contact with the emitter and butted contact with the base and collector regions which come in abutment with a trench. With the latter contacts, the studs are partly overlying the adjacent polyimide-filled trench. This results in a significant increase of the density of devices integrated in the wafer and in addition allows to have a more tolerant process from a misregistration point of view.

Detailed Description Text (16):
Baking the structure at 230.degree. C. during 30 min. is recommended, to bake-out any absorbed solvents from the polyimide trench fill, due to lift-off chemicals.

Detailed Description Text (21):
The purpose of this step is to roughly planarize the insulator topography and to expose the top of the highest contact stud. The wafer is pre-cleaned in acetone for 5 min., rinsed in de-ionized water, spin dried and then, baked in an oven at 160.degree. C. for 30 min. A photoresist material, such as AZ1350 J (diluted 5:1) is applied in order to produce a 2100 nm thick layer 30, as depicted in FIG. 6, then baked again in the same conditions as mentioned above. The photoresist is etched at approximately the same rate as that of the SiO.sub.2. AZ1350 J is appropriate in that respect,however, other materials such as polyimides may be used.

Detailed Description Text (38):
As a result of the present method of forming device metal studs in advanced technologies using the polyimide-filled deep trench isolation scheme, compatibility with advanced transistors and personalization processes, and substantial planarization are achieved. In addition, yield related problems associated with metal thinning at trench edges and parasitic FETs are resolved. Finally, a major reduction in the land capacitance of the first level interconnection metal will provide significant, additional performance enhancement to circuit types such as, for example, TTL and DTL.

CLAIMS:

1. The method for making device metal contact studs to desired contact regions of an organic material-filled deep trench isolated semiconductor device passivated by a first dielectric layer according to a determined pattern exposing at least the desired regions of the structure where the studs are to be made, said method comprising the steps of

(a) applying a lift-off mask exposing said desired regions including at least one contact region abutting a trench, without attacking said organic fill,

(b) blanket depositing the stud forming metal onto the whole structure,

(c) lifting off said mask and the overlying metal,

(d) blanket depositing a second dielectric layer onto the whole structure, the thickness of said second layer being approximately the same as the stud height,

(e) removing said second dielectric layer until the top surface of the highest contact stud is exposed and

(f) polishing both the metal and said second dielectric layer to leave a substantially planarized structure ready for further personalization.

9. The method of claim 1 wherein step (b) is followed by the step of baking the structure to bake out any absorbed solvents from the organic trench fill.

Previous Doc Next Doc Go to Doc#

L8: Entry 55 of 70 File: USPT Sep 1, 1992

DOCUMENT-IDENTIFIER: US 5143855 A
TITLE: Method for making contact openings in color image sensor passivation layer

Detailed Description Text (3):
Shown in FIG. 3a is an almost completed image sensor structure having photosensing elements 1. The bonding pad areas 2 are part of the wiring pattern and are used to connect the wiring pattern to external electronic circuits. The bonding pads are usually made of aluminum or one of its alloys, although other materials may also be used. The passivation layer 3 is grown or deposited over the entire device and may be composed of a layer or layers of silicon oxide or silicon oxynitride that may contain dopants such as boron, phosphorous, etc. This layer serves to protect the sensor from physical damage and from metallic and other contaminants.

Detailed Description Text (14):
Several photoresist solvent removal systems have been used successfully and some examples follow: Cyclohexanone (boiling point 153.degree. C.) by itself will remove most photoresist coatings and will dry slowly enough that the color filters are unaffected. In some cases, depending on the composition of the color filters, it may be possible to use NMP. However, the high boiling point (202.degree. C.) of NMP sometimes makes it difficult to dry the substrate in a reasonable amount of time; in order to decrease processing time by speeding up the rate of drying, the NMP rinse can be followed by a water rinse. Acetone (boiling point 56.degree. C.) can cause cracking and hazing of the color filter surface, but this effect can be minimized if the acetone rinse is followed immediately by a rinse with a miscible, higher boiling point solvent (e.g., water) in order to retard the rate of drying. Solvent mixtures may also be used. For example, while n-butanol has been observed to cause cracking of color filters in some instances, mixtures of n-butanol with a miscible, higher boiling point solvent in which the photoresist does not necessarily have to be soluble, e.g., xylene (boiling point 140.degree. C.), can still successfully remove the photoresist while not attacking the color filter. Concentrations of n-butanol as low as 10% have been used, but it is preferred to use a slightly higher concentration (.gtoreq.20%) so that the photoresist will dissolve quickly.

L2: Entry 23 of 26 File: USPT Jul 5, 1977

DOCUMENT-IDENTIFIER: US 4033788 A
TITLE: Ion implanted gallium arsenide semiconductor devices fabricated in semi-insulating gallium arsenide substrates

Detailed Description Text (21):
Referring now to FIG. 6, there is illustrated a process whereby a novel Schottky-barrier-gate field effect transistor is fabricated. For the particular GaAs FET device which has been successfully reduced to practice, the GaAs chromium-doped substrate 82 had a bulk resistivity of 10.sup.8 ohm centimeters, a chromium concentration of at least 10.sup.16 atoms/cc and it was approximately 18 mils in thickness. The GaAs substrate 82 in FIG. 6(a) was initially placed in a Teflon etch basket and soaked in hydrofluoric acid, HF, from between 3 and 5 minutes. Next the substrate 82 was rinsed in deionized water for approximately 5 minutes, whereafter it was removed to a hot acetone rinse and there left for approximately 15 seconds. This hot acetone rinse was maintained between 50.degree. and 55.degree. C. Next, the wafer 82 was placed in a hot solvent mixture of one-third thichloroethylene, one-third acetone, and one-third methanol for approximately 15 seconds. This latter rinse was maintained from between 50.degree. and 55.degree. C. Then the substrate 82 was again rinsed in hot 55.degree. C. acetone for approximately 15 seconds, whereafter it was transferred to a hot isopropyl alcohol bath at between 65.degree. and 70.degree. C. where it was again rinsed. The wafer 82 was then scrubbed with a soft swab which had previously been immersed in isopropyl alcohol. Next, the wafer 82 was again rinsed in hot isopropyl alcohol at 70.degree. C. for approximately 1 minute, whereafter it was blown dry with filtered dry nitrogen and then allowed to bake in a furnace at approximately 140.degree. C. for a minimum of 1 hour.

Detailed Description Text (31):
When the transistors were cooled to the 4.degree.-10.degree. K temperature range, relatively little change occured in their operating characteristics, except that gate leakage current was decreased to less than 10.sup.12 amps. This behaviour was expected because s.sup.+ dopant ions produce a very shallow energy level in GaAS (.perspectiveto.0.002 eV below the conduction band). Hence, there is negligible carrier freezout even at 4.degree. K. At temperatures below about 60.degree. K., hysteresis loops in the output characteristics disappear, as carriers are "frozen" into the trapping states with detrapping times too long to allow response to the 120 Hz sweep frequency of the curve tracer used in testing these devices. This is significant because it suggests that these Schottky-gate devices can be used as amplifiers at cryogenic temperatures and at low frequencies without detrimental effects of the deep centers.

L2: Entry 24 of 26 File: USPT Mar 2, 1976

DOCUMENT-IDENTIFIER: US 3940847 A
TITLE: Method of fabricating ion implanted znse p-n junction devices

Drawing Description Text (3):
FIG. 2 shows schematically the dopant ion beam producing the p-layer;

Detailed Description Text (5):
Prior to implantation, each substrate embodiment 20, as shown in FIG. 1, is mechanically polished on the surface 21 of the (110) crystal plane on which the p-type layer is to be formed and chemically etched on both this surface and the opposite surface 22, (also a (110) crystal plane). A suitable etching solution is two parts H.sub.2 SO.sub.4 and three parts aqueous solution of K.sub.2 Cr.sub.2 O.sub.7. Approximately 1 minute of etching at a temperature of 70.degree. to 90.degree.C has been found to be generally preferable. It is not critical. The temperature determines only the rate of the etching. Following the etching of the surfaces, the substrate elements are rinsed in a boiling 25 percent (by weight) solution of NaOH for approximately 20 seconds, then successively rinsed in boiling trichloroethylene, acetone, boiling methanol, and deionized water.

Detailed Description Text (6):
As shown in FIG. 2 the phosphorus dopant ion beam 23 forms a p-type layer 24 in the crystal. The ion implantation process is well known. A typical conventional ion implantation apparatus is shown in FIG. 5. The ions are formed in the ion source 51, accelerated in the accelerator 52, passed through the mass separator 53, and swept by the beam sweeping section 54 which directs them into the multiple heated target chamber 55 in which they implant on the enclosed specimen 56.

CLAIMS:

2. A method of fabricating a P-N junction semiconductor device in an aluminum doped n-type ZnSe single crystal having a first (110) plane surface and a second (110) plane surface comprising the steps of:

a. heat treating the said crystal in molten zinc for approximately 24 hours at a temperature of approximately 900.degree.C;

b. mechanically polishing the said first surface;

c. etching both the said first and second surfaces in two parts H.sub.2 SO.sub.4 and three parts K.sub.2 Cr.sub.2 O.sub.7 for approximately one minute at a temperature within the range of 70.degree.C to 90.degree.C;

d. rinsing the said crystal in approximately 25 percent by weight solution of boiling NaOH for approximately twenty seconds;

e. rinsing the said crystal in boiling trichloroethylene;

f. rinsing the said crystal in acetone;

g. rinsing the said crystal in boiling methanol;

h. rinsing the said crystal in deionized water;

i. implanting a p-type layer on the said first surface at room temperature by directing a phosphorus ion beam having an energy level within the range of 70 keV to 500 keV with dosages within the range from 10.sup.16 to 10.sup.14 per square centimeter;

j. annealing the said crystal at a temperature within the range of 400.degree. centigrade to 650.degree. centigrade for a time within the range of five to ten minutes;

k. depositing a gold electrical contract on the said implanted p-type layer on the first surface by sputtering or evaporation; and

l. ultrasonic soldering an indium electrical contact to the said second surface.

Previous Doc Next Doc Go to Doc#

L2: Entry 26 of 26 File: USPT Oct 14, 1975

DOCUMENT-IDENTIFIER: US 3912546 A
TITLE: Enhancement mode, Schottky-barrier gate gallium arsenide field effect transistor

Detailed Description Text (2):
Referring now to FIG. 1, there is illustrated a process whereby a novel Schottky-barrier-gate enhancement mode field effect transistor is fabricated. For the particular GaAs FET device which has been successfully reduced to practice, the GaAs chromium-doped substrate 12 had a bulk resistivity of 10.sup.8 ohm centimeters, a chromium concentration of at least 10.sup.16 atoms/ cc and it was approximately 18 mils in thickness. The GaAs substrate 12 in FIG. 1a was initially placed in a Teflon etch basket and soaked in hydroflouric acid, HF, from between 3 and 5 minutes. Next the substrate 12 was rinsed in deionized water for approximately 5 minutes, whereafter it was removed to a hot acetone rinse and there left for approximately 15 seconds. This hot acetone rinse was maintained betwen 50.degree. and 55.degree.C. Next, the wafer 12 was placed in a hot solvent mixture of one-third trichloroethylene, one-third acetone, and one-third methanol for approximately 15 seconds. This latter rinse was maintained from between 50.degree. and 55.degree.C.

Detailed Description Text (3):
Then the substrate 12 was again rinsed in hot 55.degree.C acetone for approximately 15 seconds, whereafter it was transferred to a hot isopropyl alcohol bath at between 65.degree. and 70.degree.C where it was again rinsed. The wafer 12 was then scrubbed with a soft swab which had previously been immersed in isopropyl alcohol. Next, the wafer 12 was again rinsed in hot isopropyl alcohol at 70.degree.C for approximately 1 minute, whereafter it was blown dry with filtered dry nitrogen and then allowed to bake in a furnace at approximately 140.degree.C for a minimum of 1 hour.

CLAIMS:

4. The process defined in claim 1 wherein said FET channel layer is treated by initially implanting dopant ions therein to increase the carrier concentration therein to approximately 10.sup.18 carriers per cubic centimeter, and by thereafter bombarding said layer between said source and drain electrodes with protons to controllably decrease the carrier concentration therein to approximately 10.sup.15 carriers per cubic centimeters.